Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of the claims in the application:

Listing of Claims:

1. (Original) A method for producing a packaged integrated circuit, the method comprising:

building an integrated circuit having at least one micro-structure suspended above a micro-cavity and having a heating element on said at least one micro-structure capable of heating itself and its immediate surroundings;

depositing a layer of protective material on said micro-structure such that at least a top surface of said micro-structure and an opening of said micro-cavity is covered, wherein said protective material is in a solid state at room temperature and can protect said micro-structure during silicon wafer dicing procedures and subsequent packaging, and wherein said micro-structure, said micro-cavity, and said protective material provide an unobstructed volume above and below said micro-structure after said micro-structure is subjected to a heat source;

packaging said integrated circuit; and

passing an electric current through said heating element to generate said heat source to provide said unobstructed volume above and below said micro-structure.

2. (Original) A method as claimed in claim 1, wherein said building an integrated circuit comprises providing a trimmable resistor on said micro-structure, and wherein said trimmable resistor is trimmed by said passing an electric current through said heating element.

3. (Original) A method as claimed in claim 2, wherein said trimmable resistor is said heating element, and said electric current is applied directly to said trimmable resistor.

4. (previously presented) A method as claimed in claim 1, wherein said depositing a layer of protective material comprises depositing a liquid material that becomes solid at room temperature.

5. (previously presented) A method as claimed in claim 1, wherein said depositing a layer of protective material comprises depositing a photosensitive material.

6. (previously presented) A method as claimed in claim 1, wherein said depositing a layer of protective material comprises depositing a foamed material.

7. (previously presented) A method as claimed in claim 1, wherein said depositing a layer of protective material comprises depositing a material that will shrink away from said micro-structure when receiving heat from said micro-structure as a result of said micro-structure being subjected to said heat source.

8. (Original) A method as claimed in claim 7, wherein said depositing a material that will shrink comprises depositing a porous material, and wherein a burned portion of said material dissipates among adjacent voids in unburned portions of said protective material.

9. (Original) A method as claimed in claim 8, wherein said porous material is epoxy based.

10. (previously presented) A method as claimed in claim 1, wherein said depositing a layer of protective material comprises depositing a material that will deform in response to gas pressure from a portion of said material becoming gaseous as a result of said micro-structure being subjected to said heat.

11. (Original) A method as claimed in claim 10, wherein said depositing a layer of protective material comprises depositing a material that has a high surface tension, such that said micro-cavity remains unfilled by said material.

12. (previously presented) A method as claimed in claim 1, wherein said building an integrated circuit comprises providing a micro-resonator as said micro-structure.

13. (previously presented) A method as claimed in claim 1, wherein building an integrated circuit comprises providing a plurality of micro-structures suspended above said micro-cavity.

14. (Original) A method as claimed in claim 13, wherein each of said plurality of micro-structures has a heating element residing thereon and said passing an electric current comprises passing an electric current through said heating element on each of said plurality of microstructures.

15. (Original) A method as claimed in claim 14, wherein said passing an electric current through said heating element comprises passing an electric current simultaneously through said heating element on each of said plurality of micro-structures.

16. (Original) A system for producing an integrated circuit, said system comprising:

a substrate having at least one micro-structure suspended above a micro-cavity and having a heating element on said at least one micro-structure capable of heating itself and its immediate surroundings;

a layer of protective material on said micro-structure such that at least a top surface of said micro-structure and an opening of said micro-cavity is covered, wherein said protective material is in a solid state at room temperature and can protect the micro-structure during silicon wafer dicing procedures and subsequent packaging, and wherein said micro-structure, said micro-cavity, and said protective material provide an unobstructed volume above and below said micro-structure when said micro-structure is subjected to a heat source; and

heating circuitry for passing an electric current through said heating element to generate said heat source to provide said unobstructed volume above and below said micro-structure.

17. (Original) A system as claimed in claim 16, wherein said micro-structure comprises a trimmable resistor thereon, and said trimmable resistor can be trimmed by said passing an electric current through said heating element.

18. (Original) A system as claimed in claim 17, wherein said trimmable resistor is said heating element, and said electric current is applied directly to said trimmable resistor.

19. (canceled)

20. (previously presented) A system as claimed in claim 16, wherein said layer of protective material is a photosensitive material.

21. (previously presented) A system as claimed in claim 16, wherein said layer of protective material is a foamed material.

22. (previously presented) A system as claimed in claim 16, wherein said layer of protective material is a material that will shrink away from said micro-structure when receiving heat from said micro-structure as a result of said micro-structure being subjected to said heat source.

23. (Original) A system as claimed in claim 22, wherein said material that will shrink is a porous material, and wherein a burned portion of said material dissipates among adjacent voids in unburned portions of said protective material.

24. (Original) A system as claimed in claim 23, wherein said porous material is epoxy based.

25. (previously presented) A system as claimed in claim 16, wherein said layer of protective material is a material that will deform in response to gas pressure from a portion of said material becoming gaseous as a result of said micro-structure being subjected to said heat.

26. (previously presented) A system as claimed in claim 25, wherein said a layer of protective material has a high surface tension, such that said micro-cavity remains unfilled by said material.

27. (previously presented) A system as claimed in claim 16, wherein said micro-structure is a micro-resonator.

28. (previously presented) A system as claimed in claim 16, wherein said substrate comprises a plurality of micro-structures suspended above said micro-cavity.

29. (Original) A system as claimed in claim 28, wherein each of said plurality of micro-structures has a heating element residing thereon and said heating circuitry is for passing an electric current through said heating element on each of said plurality of micro-structures.

30. (Original) A system as claimed in claim 29, wherein said heating circuitry is for passing an electric current simultaneously through said heating element on each of said plurality of micro-structures.

31. (previously presented) A system as claimed in claim 16, wherein said heating circuitry is off-chip.

32. (currently amended) A packaged integrated circuit comprising:

a substrate having at least one micro-structure suspended above a micro-cavity;

a packaging enclosing said substrate;

a protective layer of material ~~substantially~~ filling said packaging, wherein said protective material is in a solid state at room temperature and can protect said micro-structure during silicon wafer dicing procedures and subsequent packaging; and

an unobstructed volume above said micro-structure and below said micro-structure to provide said micro-cavity.

33. (canceled)

34. (previously presented) A packaged integrated circuit as claimed in claim 32, wherein said protective layer of material is a photosensitive material.

35. (previously presented) A packaged integrated circuit as claimed in claim 32, wherein said protective layer of material is a porous material.

36. (previously presented) A packaged integrated circuit as claimed in claim 32, wherein said protective layer of material is a foamed material.

37. (previously presented) A packaged integrated circuit as claimed in claim 32, wherein said micro-structure comprises a heating element thereon capable of heating itself and its immediate surroundings, and further comprising heating circuitry for passing an electric current through said heating element to generate a heat source to provide said unobstructed volume above and below said micro-structure.

38. (Original) A packaged integrated circuit as claimed in claim 37, wherein said micro-structure comprises a trimmable resistor thereon, and said trimmable resistor can be trimmed by said electric current passed through said heating element.

39. (Original) A packaged integrated circuit as claimed in claim 38, wherein said trimmable resistor is said heating element, and said electric current is applied directly to said trimmable resistor.

40. (previously presented) A packaged integrated circuit as claimed in claim 32, wherein said substrate comprises a plurality of micro-structures suspended above said micro-cavity.

41. (Original) A packaged integrated circuit as claimed in claim 37, wherein said substrate comprises a plurality of micro-structures suspended above said micro-cavity.

42. (Original) A packaged integrated circuit as claimed in claim 41, wherein each of said plurality of micro-structures has a heating element residing thereon and said heating circuitry is for passing an electric current through said heating element on each of said plurality of micro-structures.

43. (Original) A packaged integrated circuit as claimed in claim 42, wherein said heating circuitry is for passing an electric current simultaneously through said heating element on each of said plurality of micro-structures.